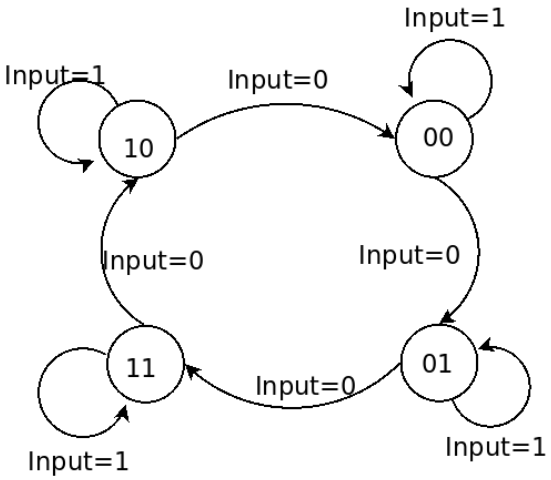
CSE/ESE 260 – Example State Machine Design and Simulation

Design a state machine that will count in gray code order (00, 01, 11, 10, 00, etc) when an input is 0 and when that input is 1, will stay in its current state.

STEP 1: State Transition Diagram
See that the 4 states are labeled, the input is shown on each path from one state to the next.



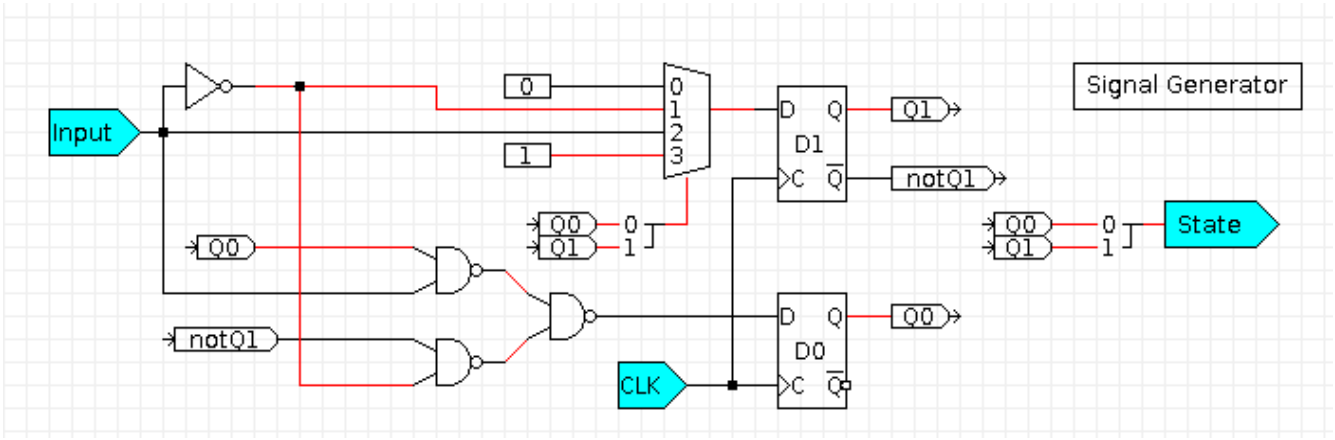
STEP 2:
Write a truth table from the input (current states Q1, Q0 and Input) to the output (in this case the next states Q1', Q0').

Q1	Q0	Input	Q1'	Q0'
0	0	0	0	1
0	0	1	0	0
0	1	0	1	1
0	1	1	0	1
1	0	0	0	0
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

STEP 3: Determine the function that represents the outputs
Canonical form:
$Q1' = \overline{Q1}\cdot Q0\cdot\overline{Input} + Q1\cdot\overline{Q0}\cdot Input + Q1\cdot Q0\cdot\overline{Input} + Q1\cdot Q0\cdot Input$
$Q0' = \overline{Q1}\cdot\overline{Q0}\cdot Input + \overline{Q1}\cdot Q0\cdot Input + \overline{Q1}\cdot Q0\cdot Input + Q1\cdot Q0\cdot Input$

These could be minimized with Kmaps or algebraically to:
$Q1' = Q0\cdot\overline{Input} + Q1\cdot Input = Q0\cdot not(Input) + Q1\cdot Input$
$Q0' = \overline{Q1}\cdot Input + Q0\cdot Input = not(Q1)\cdot not(Input) + Q0\cdot Input$

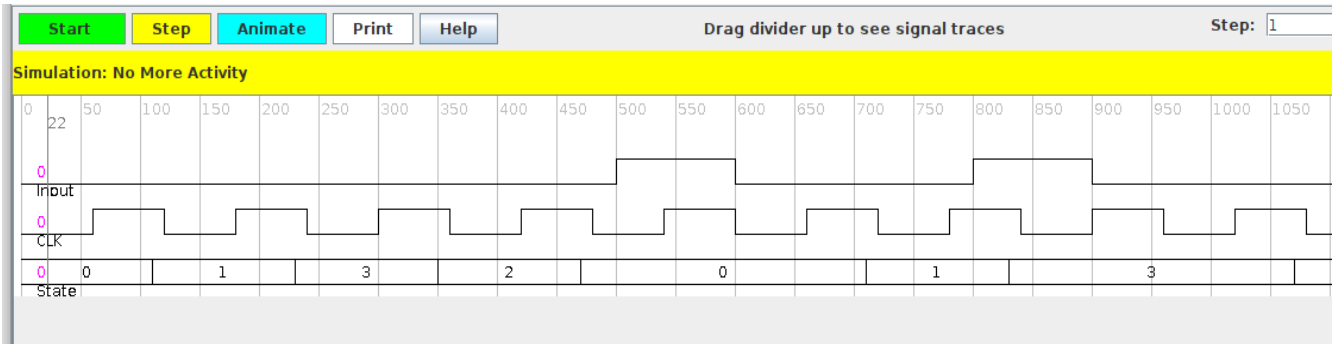
STEP 4: Synthesize the circuit (Using JLS for this)
The JLS file for this example is here:
http://feherhome.no-ip.biz/temp/wustl/260/gray_counter_example.jls



0Note:

- That there are many different ways to implement the circuit. The best implementation may vary depending upon cost, number of components and speed
- The use of named lines to reduce the number of lines that show up in the diagram

STEP 5: Simulate the circuit
In this case, the signal file is pasted below. The clock is an input in this case instead of the "Clock" signal provided by JLS. Cycle through the cases to be sure that the circuit is behaving as expected. For this simulation, the only cases not fully checked are when the input is high and the state was 1 or 2. See the simulation output below.



Note that the "Scale Factor may need to be changed to observe the entire sequence if that is desired.

Simulation used.

```
Input
0 for 500
1 for 100
0 for 200
1 for 100
0 end
CLK
0 for 60
1 for 60
0 for 60
1 for 60
```

```
0 for 60
1 for 60
0 for 60
1 for 60
0 for 60
1 for 60
0 for 60
1 for 60
0 for 60
1 for 60
0 for 60
1 for 60
0 end
```