CSE 260M / ESE 260 Intro. To Digital Logic & Computer Design

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This week

- Hw #3 Due Thursday Don't wait until the last minute!!!
 - Clarifications / Examples

Review (Again)

- Negation Notation
 - AB vs. A B
 - $\overline{A} \cdot \overline{B} = \overline{AB}$
- K-Maps: What, why, and how?

K-Maps (Again)

Review

- D Flip-Flops
 - Sequence of two D-Latches
 - Transparent at opposite clock cycles
 - Provide precise timing of data acquisition / storage
 - General focus: positive/rising edge triggers

Sequential & Synchronous Logic

- Sequential circuits
 - Can't be represented with a simple table of just inputs and outputs (Possibly a complex table of history of inputs and outputs)
 - Output depends on sequence of inputs and timing
 - Synchronous Sequential Circuits
 - Sequential circuits with additional restrictions on form to improve predictability

Synchronous Sequential Circuits

- Are synchronized by a common clock
- Uses registers (D Flip-Flops)
- Mix of registers and combinational logic
- All cycles include at least one register
- Goal: Impose predictable behavior!

Finite State Machines (FSMs)

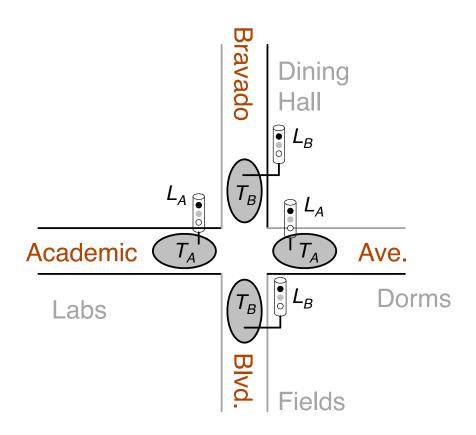
- State: A condition of being
- Finite: Er. Finite
 - Real machine has real-world limitations: $k \times D$ -latches
 - k D-Latches means $\leq 2^k$ states (finite)
- (Typically) implemented via synchronous sequential logic

FSM Applications

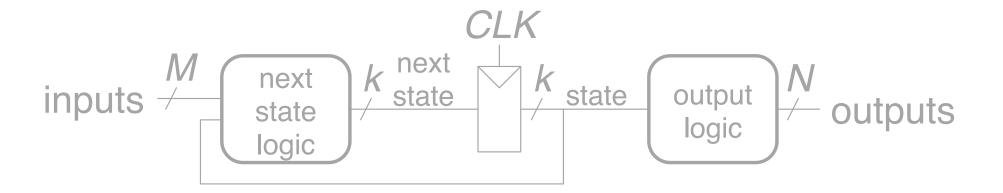
- Things with modes or sequences of steps. Examples:
 - Washing Machine (fill, agitate, rinse, spin)
 - Stop lights & Traffic control: Green, Yellow, Red
 - Locks: Locked & unlocked
 - Computer programs: Playing game vs. on menu
 - Elevator controls (state = floor)

• ...

Book Example Variation: Stop Light

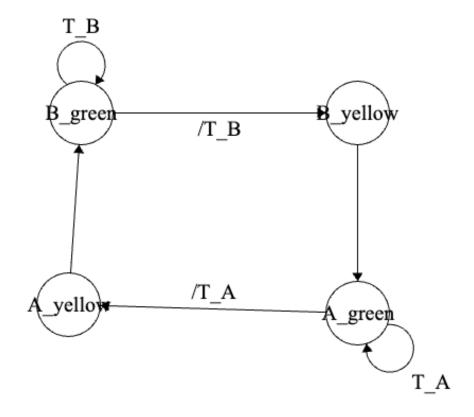


FSM: Moore Machine Structure

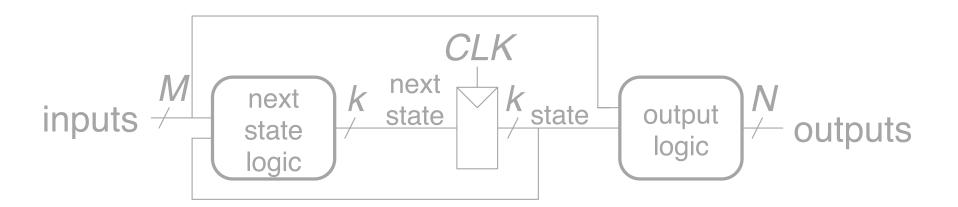


Background

- Clock is 5s: minimum time in a state
- Need to describe behavior over time
- State diagram forms
 - FSM Designer: https://wilsonem.github.io/fsm/
- Example



FSM: Mealy Machine



Next Time

- Studio
- Homework 3 due Thursday night!